

Lesson plan

Subject Name; Digital Electronics and Computer Organization

Branch: Computer Science engineering

3rd Semester(winter 2025)

Name of Faculty : Samir Kumar Sethi

Semester: 14/07/2025 To 15/11/2025

Total weeks: 15 weeks

week	Three Classes per week	Theory Topic
1 st	1 st	Overview of digital electronics, analog vs. digital systems, importance in computer engineering.
	2 nd	Number systems: Binary, Octal, Decimal, Hexadecimal; conversions between number systems.
	3 rd	Binary arithmetic: Addition, subtraction, multiplication, division; 1's and 2's complement.
2 nd	1 st	Introduction to logic gates: AND, OR, NOT, NAND, NOR, XOR, XNOR.
	2 nd	Boolean algebra: Laws, theorems, and De Morgan's theorems.
	3 rd	Simplification of Boolean expressions using Boolean algebra and Karnaugh Maps (K-Maps).
3 rd	1 st	Introduction to combinational circuits; Half Adder and Full Adder.
	2 nd	Half Subtractor and Full Subtractor.
	3 rd	Design of Multiplexers (MUX) and Demultiplexers (DEMUX).
4 th	1 st	Encoders and Decoders: Design and Applications.
	2 nd	Comparators and Parity generators/checkers.
	3 rd	Code converters: Binary to Gray, BCD to Excess-3.
5 th	1 st	Introduction to sequential circuits; difference between combinational and sequential circuits.
	2 nd	Flip-flops: SR, JK, D, and T flip-flops; truth tables and excitation tables.
	3 rd	Applications of flip-flops in counters and registers.
6 th	1 st	Counters: Synchronous and asynchronous counters; design of up/down counters.
	2 nd	Shift registers: Types (SISO, SIPO, PISO, PIPO) and applications.
	3 rd	State diagrams and state tables for sequential circuits.
7 th	1 st	Overview of computer organization; basic computer architecture (Von Neumann model).
	2 nd	Functional units of a computer: CPU, memory, input/output, and system bus.
	3 rd	Instruction cycle: Fetch, decode, execute, and store.

8 th	1 st	CPU architecture: ALU, control unit, and registers.
	2 nd	Instruction set architecture (ISA): RISC vs. CISC.
	3 rd	Addressing modes: Immediate, direct, indirect, indexed, and register addressing.
9 th	1 st	Review of digital electronics concepts (number systems, gates, circuits).
	2 nd	Review of computer organization basics (architecture, CPU).
	3 rd	Mid-term quiz or progressive assessment.
10 th	1 st	Memory hierarchy: Registers, cache, main memory, and secondary storage.
	2 nd	Types of memory: RAM, ROM, SRAM, DRAM, and their characteristics.
	3 rd	Cache memory: Mapping techniques (direct, associative, set-associative).
11 th	1 st	I/O organization: I/O modules, programmed I/O, interrupt-driven I/O.
	2 nd	Direct Memory Access (DMA) and its applications.
	3 rd	I/O interfacing: Buses, USB, and peripheral connections.
12 th	1 st	Pipelining: Concepts and benefits in CPU performance.
	2 nd	Parallel processing: Multiprocessors and multicore systems.
	3 rd	Memory management: Virtual memory and paging.
13 th	1 st	Role of digital circuits in CPU design (ALU, control unit).
	2 nd	Memory interfacing with digital circuits.
	3 rd	Case study: Designing a simple microprocessor using digital components.
14 th	1 st	Applications of digital electronics in modern computing systems.
	2 nd	Review of key concepts: Combinational/sequential circuits, CPU, memory, I/O.
	3 rd	Problem-solving session: Design and troubleshoot digital circuits.
15 th	1 st	Comprehensive review of digital electronics and computer organization.
	2 nd	Practice questions for end exam preparation.
	3 rd	Discussion of sample projects or case studies in digital systems.

Teaching Methodology

Lectures: Use slides, animations, and circuit simulations to explain concepts.

Hands-On Exercises: Use simulation tools (LT Spice, Multisim) for circuit design.

Assignments: Weekly problem sets to reinforce theoretical concepts.

Group Discussions: Encourage discussions on real-world applications.

Quizzes: Conduct periodic quizzes to assess understanding.

Case Studies: Analyze practical applications of digital electronics in computer systems.

Assessment Strategy

Progressive Assessment (30 marks):

Weekly Assignments: 5 Marks

IA-1: 10 Marks

IA-2: 10 Marks

Class participation and discussions: 5 Marks